PATENT
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	)	Docket: NVIDP008B/P000057
	)	Examiner: Vo, C.
Lindholm et al.	)	
	)	
Serial No.: N/A	)	
	)	Date: September 20, 2001
Filed: September 20, 2001	)	
	)	
For: MASKING SYSTEM AND	)	
METHOD FOR A GRAPHICS	)	
PROCESSING FRAMEWORK	)	
EMBODIED ON A SINGLE	)	
SEMICONDUCTOR PLATFORM	)	
(as amended)	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on September 20, 2001.

Signed: Erica L. Mann
Erica L. Mann

PRELIMINARY AMENDMENT

Commissioner for Patents
and Trademarks
Washington, DC 20231

Dear Sir:

Please enter the following preliminary amendments to accompany the continuation application attached hereto.

IN THE TITLE

Please delete the Title, and insert therefor:

--MASKING SYSTEM AND METHOD FOR A GRAPHICS PROCESSING FRAMEWORK EMBODIED ON A SINGLE SEMICONDUCTOR PLATFORM--

IN THE SUMMARY

Please delete the Summary, and insert therefor:

-- A graphics pipeline system with an integrated masking operation is provided. Included is a transform module adapted for being coupled to a buffer to receive graphics data therefrom. Such transform module is positioned on a single semiconductor platform for transforming the graphics data from a first space to a second space. Also included is a lighting module coupled to the transform module and positioned on the same single semiconductor platform as the transform module. The lighting modules serves for performing lighting operations on the graphics data received from the transform module. In use, a masking operation is further performed on the single semiconductor platform.

In one embodiment, the masking operation may be carried out utilizing a write mask. Moreover, the write mask may include a 2-bit write mask. In use, the masking operation may mask a write operation to a predetermined register component.

In another embodiment, the masking operation may be carried out on a bit of a control vector for allowing analysis of remaining bits of the control vector. In use, the masking operation may be capable of being used to convert vector graphics data to scalar graphics data.

In still another embodiment, the masking operation may include a color masking operation. Such masking operation may involve an ambient mask, a diffuse mask, and/or a specular mask.

In still yet another embodiment, a rasterizer may be coupled to the lighting module for rendering the graphics data received from the lighting module. Such rasterizer may be positioned on the same single semiconductor platform as the transform module and lighting module. --

IN THE SPECIFICATION

Please delete lines 7-24 on page 1, and insert therefor, -- The present application is a continuation of a parent application entitled "A Transform, Lighting and Rasterization System Embodied on a Single Semiconductor Platform," and filed December 06, 1999 under serial number 09/454,516. The present application is further related to applications entitled "Method, Apparatus and Article of Manufacture for Area Rasterization using Sense Points" which was filed on December 09, 1999 under serial number 09/455,305, and attorney docket number NVIDP005, "Method, Apparatus and Article of Manufacture for Boustrophedonic Rasterization" which was filed on December 09, 1999 under serial number 09/454,505, and attorney docket number NVIDP006, "Method, Apparatus and Article of Manufacture for Clip-less Rasterization using Line Equation-based Traversal" which was filed on December 09, 1999 under serial number 09/455,728, and attorney docket number NVIDP007, "Method, Apparatus and Article of Manufacture for a Vertex Attribute Buffer in a Graphics Processor" which was filed on December 09, 1999 under serial number 09/454,516, and attorney docket number NVIDP009, "Method, Apparatus and Article of Manufacture for a Transform Module in a Graphics Processor" which was filed on December 09, 1999 under serial number 09/456,102, and attorney docket number NVIDP010, "Method and Apparatus for a Lighting Module in a Graphics Processor" which was filed on December 09, 1999 under serial number 09/454,524, and attorney docket number NVIDP011, and "Method, Apparatus and Article of Manufacture for a Sequencer in a Transform/Lighting Module Capable of Processing Multiple Independent Execution Threads" which was filed on December 09, 1999 under serial number 09/456,104, and attorney docket number NVIDP012 which were filed concurrently herewith, and which are all incorporated herein by reference in their entirety.--

On page 8, please delete lines 8-11, and insert therefor --Figure 1 illustrates a prior art graphics processing system--.

On page 8, line 13, please delete "Figure 1B" and insert therefor --Figure 1A--.

On page 12, line 10, please delete "Figure 1B" and insert therefor --Figure 1A--.

On page 15, line 4, please delete "Figures 1 and 1A show" and insert therefor --Figure 1 shows--.

On page 15, line 4, please delete "Figures 1B" and insert therefor --Figures 1A--

On page 15, line 7, please delete "Figure 1B" and insert therefor --Figure 1A--

IN THE ABSTRACT

Please delete the Abstract, and insert therefor:

--A graphics pipeline system with an integrated masking operation is provided. Included is a transform module adapted for being coupled to a buffer to receive graphics data therefrom. Such transform module is positioned on a single semiconductor platform for transforming the graphics data from a first space to a second space. Also included is a lighting module coupled to the transform module and positioned on the same single semiconductor platform as the transform module. The lighting modules serves for performing lighting operations on the graphics data received from the transform module. In use, a masking operation is further performed on the single semiconductor platform. --

IN THE CLAIMS

Please delete claims 1-25, and add claims 26-47 as follows:

26. (New) A graphics pipeline system with an integrated masking operation, comprising:

(a) a transform module adapted for being coupled to a buffer to receive graphics data therefrom, the transform module being positioned on a single semiconductor platform for transforming the graphics data from a first space to a second space; and

(b) a lighting module coupled to the transform module and positioned on the same single semiconductor platform as the transform module for performing lighting operations on the graphics data received from the transform module;

(c) wherein a masking operation is performed on the same single semiconductor platform as the transform module and the lighting module.

27. (New) The system as recited in claim 26, wherein the masking operation is carried out utilizing a write mask.

28. (New) The system as recited in claim 27, wherein the write mask includes a 2-bit write mask.

29. (New) The system as recited in claim 28, wherein the write mask is adapted to provide control to the word level.

30. (New) The system as recited in claim 26, wherein the masking operation masks a write operation to a predetermined register component.

31. (New) The system as recited in claim 26, wherein the masking operation is carried out on a bit of a control vector for allowing analysis of remaining bits of the control vector.

32. (New) The system as recited in claim 31, wherein the masking operation is capable of being used to convert vector graphics data to scalar graphics data.

33. (New) The system as recited in claim 26, wherein the masking operation includes a color masking operation.

34. (New) The system as recited in claim 33, wherein the masking operation involves an ambient mask, a diffuse mask, and a specular mask.

35. (New) The system as recited in claim 26, and further comprising a rasterizer coupled to the lighting module for rendering the graphics data received from the lighting module, wherein the rasterizer is positioned on the same single semiconductor platform as the transform module and lighting module.

36. (New) A method for graphics processing, comprising:
(a) transforming graphics data from a first space to a second space;
(b) lighting the graphics data; and
(c) performing a masking operation on the graphics data;
(d) wherein the graphics data is transformed and lighted, and the masking operation is performed on a single semiconductor platform.

37. (New) The method as recited in claim 36, wherein the masking operation is carried out utilizing a write mask.

38. (New) The method as recited in claim 37, wherein the write mask includes a 2-bit write mask.

39. (New) The method as recited in claim 38, wherein the write mask is adapted to provide control to the word level.

40. (New) The method as recited in claim 36, wherein the masking operation masks a write operation to a predetermined register component.

41. (New) The method as recited in claim 36, wherein the masking operation is carried out on a bit of a control vector for allowing analysis of remaining bits of the control vector.

42. (New) The method as recited in claim 41, wherein the masking operation is capable of being used to convert vector graphics data to scalar graphics data.

43. (New) The method as recited in claim 36, wherein the masking operation includes a color masking operation.

44. (New) The method as recited in claim 43, wherein the masking operation involves an ambient mask, a diffuse mask, and a specular mask.

45. (New) The method as recited in claim 36, and further comprising rendering the graphics data, wherein the graphics data is rendered on the single semiconductor platform.

46. (New) A computer program product for graphics processing, comprising:

(a) computer code for transforming graphics data from a first space to a second space;

(b) computer code for lighting the graphics data; and

(c) computer code for performing a masking operation on the graphics data;

(d) wherein the graphics data is transformed and lighted, and the masking operation is performed on a single semiconductor platform.

47. (New) A system for graphics processing, comprising:

(a) means for transforming graphics data from a first space to a second space;

(b) means for lighting the graphics data; and

(c) means for performing a masking operation on the graphics data;

(d) wherein the graphics data is transformed and lighted, and the masking operation is performed on a single semiconductor platform.

REMARKS

The claims have been amended for clarifying what is claimed in the present application. At least partial support for such amendments may be found on pages 18, 30, 35-36, 39, & 48-49, and the related figures of the present application. Similar to the allowed claims of the immediate parent application, the present claims cover critical features in a novel integrated implementation on a single semiconductor platform. Simply found nowhere in the prior art are there such features uniquely implemented with a transform/lighting engine on a single semiconductor platform for affording more efficient, accelerated operation.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. If any fees are due in connection with the filing of this paper, then the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP008B). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,

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